Using Intersil's High Accuracy Real Time Clock Module

Application Note | February 28, 2008 | AN1389.0

What's an RTC?

A real time clock (RTC) is a micropower real-time clock/calendar. This device has a back-up power supply to function even when a system is off. It is separate from the CPU clock, freeing the system clock for other vital functions. RTCs are included in every electronic device that keeps track of time.

The ISL12020M provides a stable oscillation, guaranteed to ±5ppm over a wide temperature range, -40°C to +85°C. While tracking time is its primary function, an RTC can include a variety of other features to aid in system integration. The ISL12020M includes correction for daylight savings time, an alarm for one-time or periodic reminders, selectable frequency output, backup to battery or super capacitor, power fail detection, six selectable trip levels, time stamp for battery-power crossovers and 128 bytes of user SRAM—all controlled by an I^2C interface and packaged in a 20 lead DFN.

The ISL12020M can be used in electronic meters, medical appliances (Glucose meters), and telecom equipment. It is also ideal for white goods (refrigerators, washing machines) to allow delayed operation during non-peak energy usage hours. It can also be used in point-of-sale (POS) equipment to maintain reliable time and date data. In cash registers, for example, the 5ppm specification guarantees no drift greater than 12 seconds per month. That extrapolates to a maximum of 2.4 minutes per year. This high accuracy also provides reliability needed in security systems. The 1.8V minimum back-up power allows small battery or super capacitor packages to ease installation and minimize obtrusions.

What's so Special about the ISL12020M?

The benefits of the ISL12020M can be summarized in three statements:

- Embedded crystal to enable ±5ppm accuracy over the industrial temperature range
- Feature-rich—from high accuracy to alarms to power monitoring and backup systems
- Industry's smallest package—4.0mmx5.5mm DFN

Part I – The ISL12020M's Versatile Operation (Deep Features)

An RTC uses a crystal reference or, in some cases, the power line. When a crystal reference is used, 32.768kHz is common because it can be divided by simple binary counters down to 1Hz and used as a clock. This crystal is embedded in the ISL12020M package, and the pins are brought out as shown in Figure 1.

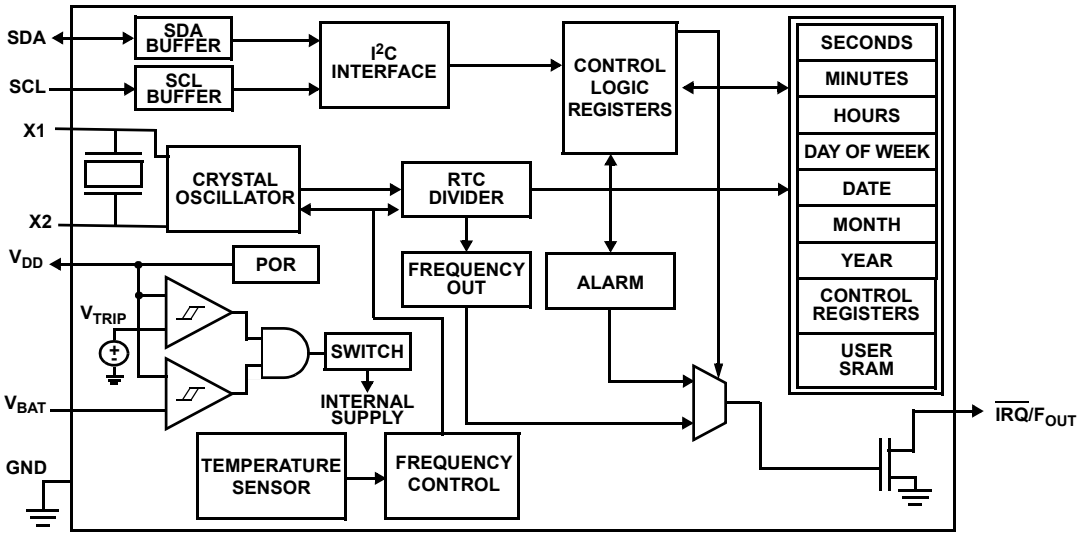

FIGURE 1. ISL12020M BLOCK DIAGRAM

Timekeeping

The ISL12020M is programmed with the I^2C serial-controlled interface at pins SDA and SCL. They pass data to the control logic registers and on to separate registers for seconds, minutes, hours, day of the week, date, month and year. The time and date information are continuously updated, corrected for shorter months and corrected for daylight savings time. The clock format is selectable for either am/pm or 24-hour (military) format. On initial power-up, the clock will not function until at least one byte is written to the clock/calendar registers.

Power Management

An integrated temperature sensor with 10-bit digital output is used by the compensation circuitry to adjust for crystal variations which change the frequency of operation.

The $\overline{IRQ}/F_{OUT}$ pin is for either hardware interrupt based on a time alarm, or clock frequency output. It can trigger on a single event (like 12am on January 1) and wait to be reset or can trigger as in interrupt mode, pulsing every time the alarm signal is flagged.

InterSeal and Reseal Operation

InterSeal is simply the ability of the device to draw zero current from the battery until the device has had V_{DD} power applied as well as V_{BAT}. If a battery is installed after product test, there will be no V_{BAT} current drain until power is applied to the V_{DD} pin.

Most product applications will have a battery installed during assembly, with no provisions to remove or disconnect after product test. After assembly, the battery would be actively powering the device while it is on the shelf. The Reseal function allows the testing procedure to set a register bit that disconnects the V_{BAT} input until the V_{DD} supply cycles OFF then ON again. This will allow zero current drain until the product is actually put into use for the first time. This will allow maximum shelf life for products that may spend a period of time idle after manufacturing and initial operation.

Alarm Operation

The alarm function generates an alarm once every minute, hour, day, week, month or year. There is one alarm register set that has essentially the same format as the clock/calendar registers. Once the alarm register matches the clock/calendar setting, an alarm flag is set in the main status register for software interrupts. The alarm can also initiate a hardware interrupt via the $\overline{IRQ}$ pin. In order for that to occur, the shared $\overline{IRQ}/F_{OUT}$ pin needs to have the frequency output disabled.

There are two alarm operation modes: Single Event and Periodic Interrupt Mode.

1. Single Event Mode is enabled by setting the ALM bit to “1”, the IM bit to “0”, and disabling the frequency output. This mode permits a one-time match between the alarm registers and the RTC registers. Once this match occurs, the $\overline{IRQ}$ output will be pulled low and will remain low until the ALM bit is reset. This can be done manually or by using the auto-reset feature.
2. Interrupt Mode (also called PIM) is enabled by setting the ALM bit to “1”, the IM bit to “1”, and disabling the frequency output. The $\overline{IRQ}$ output will now be pulsed each time an alarm occurs. This means that once the interrupt mode alarm is set, it will continue to alarm for each occurring match of the alarm and present time.

An example of interrupt mode is setting just the seconds register to “00h” and enabling the alarm and $\overline{IRQ}$ output. The the $\overline{IRQ}$ will trigger once per minute. Interrupt mode is also convenient for hourly or daily hardware interrupts in microcontroller applications such as security cameras or utility meter reading. Note that interrupt mode is NOT a timer function so exact time-out periods cannot be programmed, only RTC register matches.

However, the PIM Mode can be used for exact oscillator accuracy measurement. For example, if the seconds register only is set for alarm and PIM is enabled, then the $\overline{IRQ}$ output will be exactly 1 minute, and if a frequency counter is used to measure the pulses, the result will reflect the accuracy of the oscillator.

To clear an alarm, the ALM bit in the status register must be set to “0” with a write. Note that if the ARST bit is set to “1” (address 07h, bit 7), the ALM bit will automatically be cleared when the status register is read.

Frequency Output

The F_{OUT} pin noted on the data sheet shares pin functionality with the $\overline{IRQ}$ function. When the F_{OUT} function is enabled, the $\overline{IRQ}$ function is disabled. Four bits in the control registers (FO0 to FO3) select the functionality for this pin, as shown in Table 1. F_{OUT} ranges from 1/32Hz to 32kHz.

TABLE 1. F_{OUT} OUTPUT CONTROL

FREQUENCY (F_{OUT})	UNITS	FO3	FO2	FO1	FO0
0	Hz	0	0	0	0
32768	Hz	0	0	0	1
4096	Hz	0	0	1	0
1024	Hz	0	0	1	1
64	Hz	0	1	0	0
32	Hz	0	1	0	1
16	Hz	0	1	1	0
8	Hz	0	1	1	1
4	Hz	1	0	0	0
2	Hz	1	0	0	1
1	Hz	1	0	1	0
1/2	Hz	1	0	1	1
1/4	Hz	1	1	0	0
1/8	Hz	1	1	0	1
1/16	Hz	1	1	1	0
1/32	Hz	1	1	1	1

The F_{OUT} function can be used for clocking a low-power microcontroller in the system or as an accurate timer. The frequency output pin is an open drain and requires a pull-up resistor. For low frequency signals of <1024Hz, 50kΩ or greater values can be used. For accurate 32.768kHz clocking, a 2.2kΩ pull-up is advised. The FOBATB bit in the INT register controls whether the F_{OUT} pin is active in battery backup.

Serial Data Interface

The serial interface consists of clock and data (SCL and SDA pins) and meets the timing and pin voltage requirements of the I^2C interface. Start and stop conditions are used along with acknowledge on address and data transfers. The devices can be used with clock frequencies up to 400kHz. The SDA output is open drain and the serial bus line needs a pull-up resistor for proper operation. It is highly recommended that the serial interface pull-up resistors are tied to V_{DD} and that V_{DD} needs to go to 0V (or very close) when powered down to avoid excessive battery current drain.

The serial interface will operate down to the point of battery switchover and does not operate in battery backup mode.

Power Dissipation and Battery Backup Switchover Circuit

The power supply pin (V_{DD}) and backup-up battery pin (V_{BAT}) are compared through a pair of Schmitt triggers before being switched into the chip's supply path. In the case of a power outage, the backup battery or super capacitor assumes the responsibility of powering the system (see Figure 2). The ISL12020M makes this switch automatically. V_{DD} switches to V_{BAT} at the lower of either V_{TRIP} or V_{BAT}, with hysteresis for glitch rejection (see Figure 2). There is approximately 50mV of hysteresis in the voltage comparator when switching from V_{DD} to V_{BAT}, and 50mV when switching from V_{BAT} to V_{DD}.

Power failure detection has 6 programmable levels to customize the brownout detection level for the user's system. The battery status monitors have 7 levels, also user-selectable, which report the voltage level of the battery to warn if the charge is almost depleted. The system keeps a time stamp for the first power to backup and the last backup to power crossovers, giving the user an idea of the time frame of power outages.

The supply voltage can range from 2.7V to 5.5V while the backup supply voltage can range from 1.8V to 5.5V. The ISL12020M consumes 4µA of current with a 5V supply. That power rises to approximately 300µA during I^2C communications. During battery back-up mode, only 1µA is consumed at 3V. During a temperature conversion cycle, the supply current is about 120µA, but this only occurs for about 60ms every minute, therefore it doesn't affect the overall power consumption.

The I^2C interface and non-essential features are shut down in battery mode to preserve backup power—only the clock/calendar and SRAM receive power in this state.

If the V_{BAT} input is not used, it should be tied to ground, not to V_{DD}.

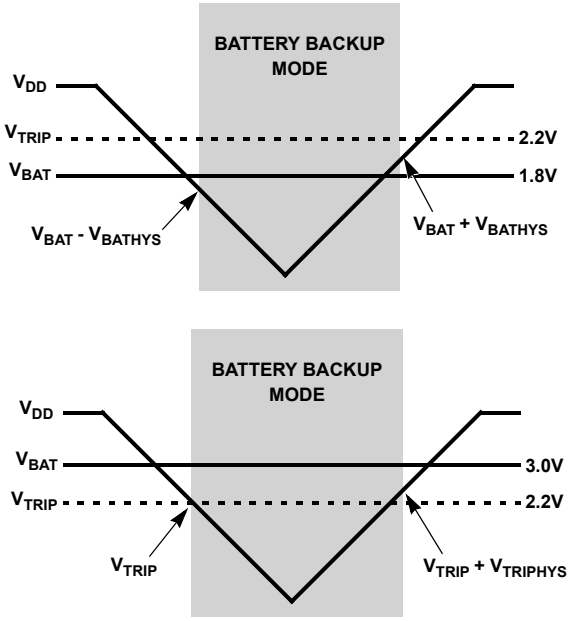

FIGURE 2. BATTERY SWITCHOVER WHEN $V_{BAT} < V_{TRIP}$ (TOP) AND $V_{BAT} > V_{TRIP}$ (BOTTOM)

V_{DD} Ramp Rates and Glitch Detection

The data sheet specifies a -10V/ms maximum negative slew rate (power-down V_{DD} ramp rate). This should be followed to avoid losing any of the RAM register settings during power-down. If the negative slew rate is excessive, then the internal power node voltages can droop during switchover, causing the SRAM cells to change state or erase. In most systems this is not an issue, but the V_{DD} power-down waveform should be observed as a precaution.

If the V_{DD} power-down timing is exceedingly fast, a simple fix is to add an RC network to the V_{DD} pin. Since the supply current for the device is very low, series resistance of up to 1kΩ can be added, and choice of a capacitor value is left to the designer. Typically, 0.47µF can be used but lower values are possible—depending on the existing V_{DD} slew rate.

The V_{DD}/V_{BAT} power circuit also contains a glitch detection circuit to protect from incorrect serial bus writes after a brownout situation. This circuit disables the serial bus for about 90ms following the power-up. To trigger the delay, the V_{DD} must drop below the battery trip point yet stay above approximately 1.0V (limit of active circuit operation). After that, the power-up ramp must be slower than 0.25V/ms to trigger the delay. To be safe, serial interface software may need to consider the 90ms delay in all power-up routines.

Battery Backup Details

Many types of batteries can be used with the Intersil RTC products. 3.0V or 3.6V Lithium batteries are appropriate, and sizes are available that can power an Intersil RTC device for up to 10 years. Another option is to use a super capacitor for applications where V_{DD} may disappear intermittently for short periods of time. Depending on the value of super capacitor used, backup time can last from a few days to two weeks (with >1F). A simple silicon or Schottky barrier diode can be used in series with V_{DD} to charge the super capacitor, which is connected to the V_{BAT} pin (see Figure 3). Try to use Schottky diodes with very low leakages, <10nA is desirable. Do not use the diode connection to charge a battery (especially lithium batteries!). Note that if a lithium coin cell is inserted into a holder after a board has been tested and powered down, then the InterSeal function will prevent any battery drain until it is first powered up in actual use.

Super Capacitor Backup

A super capacitor can be used as an alternative to a battery in cases where shorter backup times are required. Since the battery backup supply current required by the ISL12020M is extremely low, it is possible to get months of backup operation using a super capacitor. Typical capacitor values are a few µF to 1F or more, depending on the application.

If backup is only needed for a few minutes, than a small inexpensive electrolytic capacitor can be used. For extended periods, a low leakage, high capacity super capacitor is the best choice. These devices are available from vendors such as Panasonic and Murata. The main specifications include working voltage and leakage current. A capacitor with a working voltage of 5.0V may have a reduced lifetime if the supply voltage is slightly high. The leakage current should be as small as possible—well below 1µA. A standard electrolytic capacitor with DC leakage current in the microamps will have a severely shortened backup time.

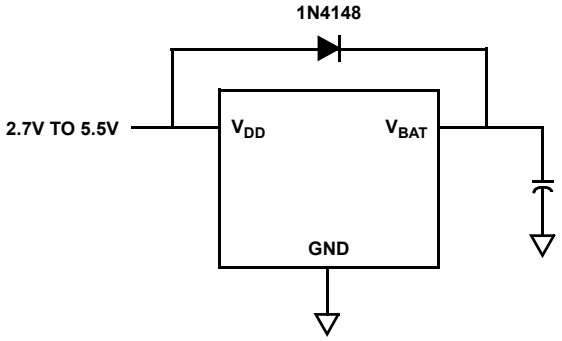

FIGURE 3. SUPER CAPACITOR CHARGING CIRCUIT

Part II – High Accuracy Temperature Compensated Oscillator

The typical 32.768kHz crystal has an accuracy characteristic that is similar to that shown in Figure 4. There is a turnover temperature (T_0) at the apex where the accuracy falls off at higher or lower temperatures. The shape is parabolic as it varies with the square of the difference between the actual temperature and the turnover temperature is:

$$\text{ERROR} = \alpha \times (T - T_0), \text{ppm} \quad \text{(EQ. 1)}$$

where α is a constant for the crystal type, and for 32.768kHz crystals, is typically 0.034ppm/°C.

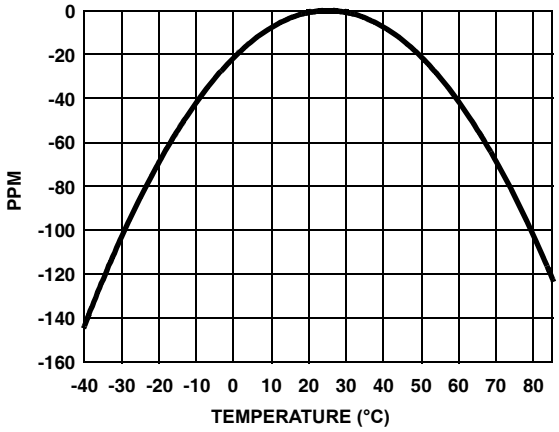

FIGURE 4. RTC CRYSTAL TEMPERATURE DRIFT

Crystal Included in ISL12020M

The ISL12020M module, however, uses an **embedded** crystal. The temperature compensation circuitry inside the ISL12020M performs the job of measuring temperature, and then compensating for this crystal error curvature. The compensation parameters for each device are determined at production test and programmed into the device. At initial power-up, those parameters are recalled to active registers and are then used by the compensation circuitry. The accuracy improvement enables the ISL12020M to provide at most ±5ppm error from ideal over the full -40°C to +85°C range of temperatures.

A graph of the frequency output versus temperature for 4 ISL12020M RTCs appear in Figure 5. These devices contained trimmed compensation values from production testing. The error over temperature has now been reduced greatly and the value of F_{OUT} remains well within the ±5ppm tolerance over temperature.

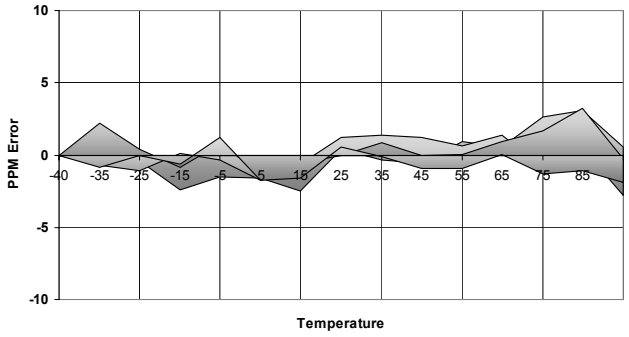

FIGURE 5. TRIMMED PACKAGE OUTPUT FREQUENCY (ppm) OVER TEMPERATURE (°C) WITH V_{DD} = 2.7V (4 DEVICES)

Active Temperature Compensation Operation

The ISL12020M compensation circuitry is an intelligent logic circuit which takes the temperature sensor digital value as the only input variable. Two different adjustment mechanisms are used, Analog Trimming (AT) for 1ppm fine adjustment resolution, and Digital Trimming (DT) for coarse adjustment.

A precision temperature sensor provides a digital temperature code, used by the compensation circuitry for correction. The sensor has a tight ±2°C accuracy and the digital value is accessible by the I^2C interface in a register.

There are also registers which contain values for the parameters α (alpha) and T_0, as mentioned above. There are separate register for the cold and hot alpha constants (ALPHA and ALP_H, respectively). There is also a register for step size adjustment (BETA) to insure the AT trimming is close to 1ppm per bit. Finally, an initial trimming register (ITR0) contains values for initial AT and DT trimming to insure the device is very close to 0ppm error at the T_0 temperature.

The compensation circuitry then uses the register values for the crystal constants alpha and T_0, and combines those with the calibration from the BETA and ITR0 registers to produce “Final” values for the AT and DT, known as FATR (Final AT Resister) and FDTR (Final DT register). Those AT and DT values combine to directly compensate for the frequency error at a given temperature.

The temperature sensor produces a new value every 60 seconds (or up to 10 minutes in battery mode), which triggers the logic to calculate a new AT/DT value set. For every temperature calculation result, there can only be one corresponding AT/DT correction value.

Using the ISL12020M

Layout Considerations

The crystal pin at X1 has a very high impedance, and oscillator circuits operating at low frequencies (such as 32.768kHz) are known to pick up noise very easily if layout precautions are not followed. Most instances of erratic clocking or large accuracy errors can be traced to the susceptibility of the oscillator circuit to interference from adjacent high speed clock or data lines. Careful layout of the RTC circuit will avoid noise pickup and ensure accurate clocking. Figure 6 shows a suggested layout for the ISL12020M device. Three main precautions should be followed:

- Do not run the serial bus lines or any high speed logic lines in the vicinity of the X1 and X2 pins. These logic level lines can induce noise in the oscillator circuit, causing misclocking.
- Add a ground trace around the device with one end terminated at the chip ground. This guard ring will provide termination for emitted noise in the vicinity of the RTC device.
- Do not run a ground plane immediately under the RTC. This will add capacitance to the X1/X2 pins and change the trimmed frequency of the oscillator. Instead, try to leave a gap in any planes under the RTC device.

The best way to run clock lines around the RTC is to stay outside of the ground ring by at least 2 millimeters. Also, use the V_{BAT} and V_{DD} as guard ring lines as well, they can isolate clock lines from the X1 and X2 pins. In addition, it is a good idea to avoid a ground plane under the X1 and X2 pins of the device, as this will affect the load capacitance and therefore the oscillator accuracy of the circuit. If the $\overline{IRQ}/F_{OUT}$ pin is used as a clock, it should be routed away from the RTC device as well. The traces for the V_{BAT} and V_{DD} pins can be treated as a ground, and should be routed closely around the device.

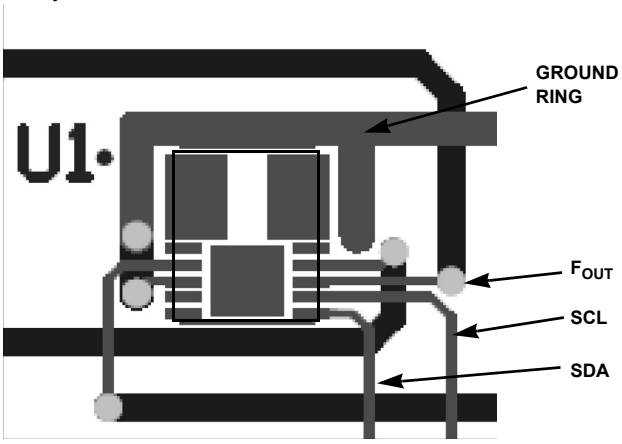

FIGURE 6. SUGGESTED LAYOUT FOR ISL12020M

Measuring Oscillator Frequency Accuracy

Initial accuracy is best adjusted by enabling the frequency output (using the INT register, address 08h), and monitoring the $\overline{IRQ}/F_{OUT}$ pin with a calibrated frequency counter. (Note: DO NOT use a scope probe on the X2 pin to monitor the oscillator waveform for this purpose. Even with a low capacitance probe, there will be accuracy error induced.)

The 1Hz frequency option is the easiest to monitor. The gating time should be set long enough to ensure accuracy to at least 1ppm. The IATR register should be set to the center position, or 100000b, to begin with. Once the initial measurement is made, then the IATR register can be changed to adjust the frequency. Note that increasing the IATR register for increased capacitance will lower the frequency, and vice-versa. Note that most crystals will have tight enough initial accuracy at room temperature so that a small IATR register adjustment (with no IDTR) should be all that is needed.

Measuring Oscillator Accuracy

The best way to analyze the ISL12020M frequency accuracy is to set the $\overline{IRQ}/F_{OUT}$ pin for a specific frequency, and look at the output of that pin on a high accuracy frequency counter (at least 7 digits accuracy). Note that the $\overline{IRQ}/F_{OUT}$ is an open drain output and will require a pull-up resistor. Using the 1.0Hz output frequency is the most convenient as the ppm error is just:

$$ERROR = (F_{OUT} - 1) \times 10^6, ppm \quad \text{(EQ. 2)}$$

Other frequencies may be used for measurement but the error calculation becomes more complex. When the proper layout guidelines above are observed, the oscillator should start up in most circuits in less than one second. Some circuits may take slightly longer, but start-up should definitely occur in less than 3 seconds.

Temperature Compensation Operation

The ISL12020M temperature compensation feature needs to be enabled through I^2C communication after initial power-up. This must be done in a specific order as follows:

1. Read register 0Dh, the BETA register. This register contains the 5-bit BETA trimmed value which is automatically loaded on initial power-up. Mask off these 5 LSB's of the value, just read the remaining bits.
2. Bit 7 of the BETA register is the master enable control for temperature sense operation. Set this to "1" to allow continuous temperature frequency correction. Frequency correction will then happen every 60s with V_{DD} applied.
3. Bits 5 and 6 of the BETA register control temperature compensation in battery backup mode. Set the values for the operation desired.
4. Write back to register 0Dh making sure not to change the 5 LSB values, and include the desired compensation control bits.

Note that every time the BETA register is written with the TSE bit = 1, a temperature compensation cycle is instigated and a new correction value will be loaded into the FATR/FDTR registers (if the temperature changed since the last conversion).

Also note that registers 0Bh and 0Ch, the ITR0 and ALPHA registers, should not be changed. If they must be written, be sure to write the same values that are recalled from initial power-up. The ITR0 register may be written if the user wishes to control the frequency of the oscillator at room temperature for test or monitoring purposes. The original recalled value should always be re-written after such testing.